CALIBRATION SCHEME FOR LOGARITHMIC IMAGE SENSOR

Field of the Invention

[0001] The present invention relates to electronics, and in particular, to a solid-state image sensor.

Background of the Invention

[0002] Dynamic range is a very important parameter of any imaging system. Human vision has the capability to see details across a wide illumination range in a single scene, and is reported to exhibit around 200dB of dynamic range. Scenes in excess of 100dB are not uncommon in everyday situations. Consequently, designers of CMOS and CCD image sensors are continuously looking for ways to increase dynamic range.

[0003] Sensors having logarithmic characteristics have been used to image scenes of high dynamic range. In a logarithmic mode the pixel voltage is continuously available and no integration time is used. In a typical CMOS arrangement, the induced photocurrent flows through one or more MOS transistors and sets up a gate-source voltage that is proportional to the logarithm of the photocurrent. This is shown in Figure 1 where the gate-source voltage appears across the device M2. Since the photocurrent is very small, the MOS device(s) will operate in a sub-threshold, and the voltage varies

logarithmically with the photocurrent. The voltage is read out by source follower circuitry. Around six decades of light can be captured in the logarithmic mode.

[0004] Due to the small size of the devices used in the pixels, a high degree of mismatch results from process variations, and produces fixed pattern noise (FPN) across the array. Logarithmic sensors cannot use double sampling (in its conventional form) for mismatch removal since this technique only removes the variation of the device M1 and does not alter the effect of device M2. This arises from the fact that the logarithmic architecture operates continuously in time and has no reference state.

[0005] Another disadvantage of the logarithmic arrangement is a slow response time for low light levels. Increased photocurrent for a given light level can be accomplished by increasing the size of the light sensing element, but this is not desirable since the cost for a given resolution will increase accordingly.

[0006] Calibrating the pixels addresses the FPN problem, that is, by bringing them into a reference state so that the FPN can be learned and then cancelled. The common way to calibrate a logarithmic pixel on-chip is to pull a matched current through the load device of each pixel using a current source in each column. This places the pixel into a known reference state that should be equivalent to illuminating the sensor with a uniform intensity. However, this requires an extra vertical line in each column for the current source, and the associated capacitance of the extra line prevents small calibration currents from settling quickly.

[0007] U.S. Patent No. 6,355,965 to He et al. shows an arrangement in which a calibration access transistor shorts the source follower, and the calibration is performed without the need for an extra vertical line. But this still has problems of a long settling time for low photocurrents.

[0008] Kavadias discloses in the article "A Logarithmic Response CMOS Image Sensor With On-Chip Calibration", IEEE Journal of solid-state circuits, vol. 35, No. 8, August 2000, a high calibration current being pulled through the load device. This disclosure uses an NMOS transistor and capacitor in a column instead of a constant current source. The calibration point can therefore be far from the operating point of the pixel due to the difference between photo and calibration currents.

[0009] Loose et al. discloses in the article "A Self-Calibrating Single-Chip CMOS Camera with Logarithmic Response", IEEE Journal of solid-state circuits, vol. 36, No. 4, April 2001, a correction voltage being stored in an analog memory (a capacitor) in the pixel such that the signal voltage is free from offsets. The entire amplifier is in the column, and an extra vertical line is used to access the current source.

Summary of the Invention

[00010] The invention provides an image sensor as defined in claim 1, and a method of calibrating an image sensor as defined in claim 10. Preferred features and advantages of the invention will be apparent from the other claims and from the following description.

Brief Description of the Drawings

[00011] An embodiment of the invention will now be described, by way of example only, with reference to the drawings, in which:

[00012] Figure 1 is a schematic diagram of a pixel in an image sensor according to the prior art; and

[00013] Figure 2 is a schematic diagram of a pixel in an image sensor forming one example of the present invention.

Detailed Description of the Preferred Embodiments

[00014] Referring to Figure 2, a pixel has a photodiode P which causes a photocurrent to flow through device M2, thus causing it to operate in a sub-threshold (assuming device M5 is on). The photodiode voltage at the node pix is used as the inverting input to amplifier A. The non-inverting input receives a reference voltage Vref. The node pix will be held at the reference voltage Vref (plus the offset of the amplifier) and the logarithmic result will be available at the output of the amplifier A.

[00015] To calibrate the pixel, the node pix is isolated from the photodiode P by device M5 to eliminate the effects of the photocurrent. The reference voltage Vref is now ramped, and due to the amplifier feedback loop, the voltage at the node pix will try to track it. As the pixel voltage rises it will induce a current which must be supplied through M2.

[00016] The ramp voltage is applied to make use of the fact that a constant current can be generated if there is a constant voltage change across a constant capacitance. Using the formula $I = C*dV/dt$ and knowing

the capacitance, a voltage ramp can be programmed to produce a constant current.

[00017] In Figure 2, the capacitance of the pixel is given by the capacitance on the drain of device M5 and the gate capacitance of the inverting input of the amplifier A. If these capacitances are well matched across the array then the calibration currents will be matched.

[00018] This arrangement allows the pixels to be calibrated without the use of additional vertical lines and current sources. It also allows very small calibration currents to be produced without the settling time problems associated with current sources and vertical access lines with large capacitance.

[00019] As well as providing a calibration current, the ramping of the reference voltage Vref can be used to aid the settling time of the circuit when the device M5 is on and the logarithmic voltage is dependent on the photocurrent. The node pix is able to charge up quickly as the feedback loop will cause the device M2 to turn on more quickly and supply more current. However, the node pix can only discharge with the current supplied from the photodiode P which could be very small and cause a very long settling time. If the amplifier has any overshoot then this settling time could be a problem for low photocurrents. By ramping the reference voltage Vref the oscillations can be absorbed by the ramp and at the end of the ramping period the circuit should settle more quickly.

[00020] The amplifier can be completely within the pixel, as shown. Alternatively, the amplifier could be formed partly within the pixel and partly within the column and switched between pixels as required. The

invention thus provides an improvement in calibrating a logarithmic pixel.